RDNA Architecture
Forward-looking statement

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Highlights of the RDNA Workgroup Processor (WGP)

- Designed for lower latency and higher effective IPC
- Native Wave32 with support for Wave64 via dual-issue
- Single-cycle instruction issue
- Co-execution of transcendental arithmetic operations
- Resources of two Compute Units available to a single workgroup
- 2x scalar execution resources
- Vector memory improvements
GCN Compute Units

- 4 Compute Units:

- RX590 has 36 CU, RX Vega64 has 64 CU
### RDNA Workgroup Processors (WGP)

**2 Workgroup Processors:**

<table>
<thead>
<tr>
<th>I$</th>
<th>K$</th>
<th>SALU</th>
<th>SIMD32</th>
<th>SALU</th>
<th>SIMD32</th>
</tr>
</thead>
<tbody>
<tr>
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</tbody>
</table>

- “Navi” has 20 WGP, corresponding to 40 CU
4-cycle instruction issue on GCN

- Each wave is assigned to one SIMD16, up to 10 waves per SIMD16
- Each SIMD16 issues 1 instruction every 4 cycles
- Vector instructions throughput is 1 every 4 cycles

<table>
<thead>
<tr>
<th>Cycle</th>
<th>0</th>
<th>1</th>
<th>2</th>
<th>3</th>
<th>4</th>
<th>5</th>
<th>6</th>
<th>7</th>
</tr>
</thead>
<tbody>
<tr>
<td>SALU</td>
<td>SIMD0</td>
<td>SIMD1</td>
<td>SIMD2</td>
<td>SIMD3</td>
<td>SIMD0</td>
<td>SIMD1</td>
<td>SIMD2</td>
<td>SIMD3</td>
</tr>
<tr>
<td>SIMD0</td>
<td>0-15</td>
<td>16-31</td>
<td>32-47</td>
<td>48-63</td>
<td>0-15</td>
<td>16-31</td>
<td>32-47</td>
<td>48-63</td>
</tr>
</tbody>
</table>
Single-cycle instruction issue on RDNA

- Each wave is assigned to one SIMD32, up to 20 waves per SIMD32
- Each SIMD32 issues 1 instruction every cycle
- Vector instruction throughput is 1 every cycle (for Wave32)
- 5 cycles of latency are exposed (automatic dependency check in hardware)
  - Dependency stalls can be filled by other waves
Single-cycle instruction issue: ILP and scheduling matters

```
v_fma_f32 v4, v0, s0, s3
v_fmac_f32 v4, v1, s1
v_fma_f32 v5, v0, s4, s7
v_fmac_f32 v5, v1, s5
v_fma_f32 v6, v0, s8, s11
v_fmac_f32 v6, v1, s9
```

```
v_fma_f32 v4, v0, s0, s3
v_fma_f32 v5, v0, s4, s7
v_fma_f32 v6, v0, s8, s11
v_fmac_f32 v4, v1, s1
v_fmac_f32 v5, v1, s5
v_fmac_f32 v6, v1, s9
```
Transcendental math co-execution

- rcp/rsq/sqrt/log/exp/sin/cos
- Transcendental instructions are \( \frac{1}{4} \) rate (like GCN)
- Non-transcendental instructions can execute in parallel

```
Cycle 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
v_rcp_f32 v14, v14
v_fma_f32 v8, v0, s4, v2
v_fma_f32 v9, v1, s4, v3
v_rcp_f32 v15, v15
v_fma_f32 v10, v4, s4, v5
v_fma_f32 v11, v6, s4, v7
v_mul_f32 v8, v8, v14
v_mul_f32 v9, v9, v14
```
Instruction latency: GCN vs. RDNA

- Wave64 on GCN
  
  ```
  v_rcp_f32 v14, v14
  v_fma_f32 v8, v6, s4, v2
  v_fma_f32 v9, v1, s4, v3
  v_rcp_f32 v15, v15
  v_fma_f32 v10, v4, s4, v5
  v_fma_f32 v11, v6, s4, v7
  v_mul_f32 v8, v8, v14
  v_mul_f32 v9, v9, v14
  ```

- 2x Wave32 on RDNA – one per SIMD32
  
  ```
  v_rcp_f32 v14, v14
  v_fma_f32 v8, v6, s4, v2
  v_fma_f32 v9, v1, s4, v3
  v_rcp_f32 v15, v15
  v_fma_f32 v10, v4, s4, v5
  v_fma_f32 v11, v6, s4, v7
  v_mul_f32 v8, v8, v14
  v_mul_f32 v9, v9, v14
  ```

- With small dispatches, RDNA behaves significantly better than GCN
Vector register file (VGPRs)

- Each SIMD32 has 1024 physical registers
- Divided among waves, up to 256 each
- Wave64 "counts double"
- Examples:
  - 4x Wave32 with 256 VGPRs
  - 2x Wave64 with 256 VGPRs
  - 16x Wave32 with 64 VGPRs
  - 8x Wave64 with 64 VGPRs
- Occupancy in "# of threads per SIMD lane" is unchanged from GCN
  - Occupancy 4 on GCN = 16 threads per lane
  - RDNA equivalent: 16x Wave32 or 8x Wave64
- Call to action:
  - Think about occupancy in terms of "# of threads per SIMD lane"
Vector register-based occupancy illustrated

- GCN: Wave64, 128 VGPR allocation

- RDNA: Wave32, 128 VGPR allocation
Keeping the SIMD busy: GCN vs. RDNA

- Example: Small dispatch, 64 threads only
Keeping the SIMD busy: GCN vs. RDNA

- RDNA requires much fewer threads for all blocks to light up:
Keeping the SIMD busy: GCN vs. RDNA

- 2 CU require 2*4*64 = **512 threads** to be able to reach 100% ALU utilization
- WGP requires 4*32 = **128 threads** to be able to reach 100% ALU utilization
  - Only achieved with high instruction level parallelism (ILP)
  - Graphics workloads often have 3 independent streams (RGB / XYZ)
    - 256 threads / WGP often reach >90% ALU utilization in practice

- Additional threads are needed on both GCN and RDNA to hide memory latency
  - Unless you can fill the wait with ALU (this is extremely rare)
  - # of threads required for memory latency hiding has reduced as well, but not as much

- Fewer threads required overall to keep the machine busy
  - Utilization ramps up more quickly after barriers
  - High VGPR counts hurt slightly less

- Call to action:
  - Keep ILP in mind when writing shader code

---

1. Observed in pixel shaders in a trace of a typical game rendering workload
What **not** to do for ILP

- Naïve idea: run multiple work items in a single thread

  ```
  image_load v[0:1], ...
  s_waitcnt vmcnt(0)
  v_mul_f32 v0, v0, s0
  v_mul_f32 v1, v1, s0
  image_store v[0:1], ...
  ```

- Problems:
  - Code bloat (mind the I$ size!)
  - Higher VGPR count
  - Increases the effective dispatch granularity; more waste along the edges

- **Don't panic:** extra waves are a really good source of parallelism
Wave64 via dual-issue

- Vector instructions of Wave64 execute as 2x Wave32
- Same instructions, no code bloat

When low or high half of EXEC is 0, that half skips execution

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<td>v_fma_f32 v4, v0, s0, s3</td>
<td></td>
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</tbody>
</table>
  (high half)                  |   |   |   |   |   |   |   |   |   |   |   |   |
| v_fma_f32 v5, v0, s4, s7    |   |   |   |   |   |   |   |   |   |   |   |   |
  (high half)                  |   |   |   |   |   |   |   |   |   |   |   |   |
| v_fma_f32 v6, v0, s8, s11   |   |   |   |   |   |   |   |   |   |   |   |   |
  (high half)                  |   |   |   |   |   |   |   |   |   |   |   |   |
| v_fmac_f32 v4, v1, s1       |   |   |   |   |   |   |   |   |   |   |   |   |
  (high half)                  |   |   |   |   |   |   |   |   |   |   |   |   |
Wave32 vs. Wave64

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<th>Wave32</th>
<th>Wave64</th>
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<td>Lower latency / wave lifetime</td>
<td>Allows higher occupancy (# threads per lane)</td>
</tr>
<tr>
<td>Quicker ramp-up of WGPs after barriers</td>
<td>More efficient for attribute interpolation</td>
</tr>
<tr>
<td>More efficient for partially filled waves</td>
<td></td>
</tr>
<tr>
<td>Tighter memory access patterns</td>
<td></td>
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</tbody>
</table>

- Compiler makes the decision
  - Compute and vertex shaders usually as Wave32, pixel shaders usually as Wave64
  - Heuristics will continue to be tuned for the foreseeable future

- Call to action:
  - Make sure barriers in shaders are semantically correct!
    - The compiler removes unnecessary barriers
  - Enable variable subgroup size, especially when using wave/subgroup intrinsics (Vulkan extension pending...)
  - Workgroup size: keep it a multiple of 64
LDS per workgroup processor

- 128 kB per workgroup processor
- Shared memory for compute, attributes for pixel shaders
- Up to 64 kB per workgroup
- Read / write / atomic throughput of up to 32 dwords per cycle (doubled relative to GCN)
- 32 banks
  - Same as “Vega”
  - Mind the bank conflicts!
Additional IPC improvements

- **Overall goal**: fewer move instructions
- **Dual scalar source**

  ```
  s_buffer_load_dword x2 s[0:1], ...
  s_waitcnt lgkmcnt(0)
  v_mov_b32 v1, s0
  v_fma_f32 v0, v0, v1, s1
  ```

- **All VALU instructions support immediates (96-bit instructions)**

  ```
  s_mov_b32 s0, 0x3f490fdb ; pi/4
  v_mul_f32 v0, |v0|, s0
  ```

- **Optional NSA (non-sequential address) encoding for image instructions**
  - Avoids moves
  - Simplified register allocation helps reduce VGPR pressure

  ```
  v_mov_b32 v7, v14
  image_sample v[0:1], v[7:8], ...
  ```
Workgroup Processor summary

- Wave32 and single-cycle issue for better latency
- Co-execution of transcendental instructions
- Higher memory and LDS bandwidth, lower latency

Calls to action:

- Check your barriers!
- Enable variable subgroup sizes once API support is there
- Workgroup size: keep a multiple of 64
- Keep an eye on instruction level parallelism (ILP), but don’t panic!
- Calculate occupancy as "# threads per SIMD lane"
- Worry a little less about VGPR pressure
- Worry a little more about LDS bank conflicts
- Use ShuffleXor instead of Shuffle when possible
Recap

- Explicit APIs expose more of the nitty-gritty details
  - Barriers and what caches get flushed
  - Blocks which can’t read/write compressed data (DCC and present 😊)

- GCN was compute/throughput focused, RDNA is graphics/latency focused

- Fix many bottlenecks found over the years
  - Geometry handling
  - Reduce cache flushes
  - Less “sensitive” compared to GCN (less work in flight needed, lower latency, etc.)

- Enable a more scalable architecture
  - Pave the way for a whole family of new GPUs
  - New features, different configurations, etc. coming down the line
Memory Hierarchy

RDNA (RX 5700 XT)

- Graphics Core
- Shader Engine
- Shader Array
- WGP
- L0$ and I$ and K$
- L1$
- L2$
- Scalable Data Fabric
- HBM2

GCN (RX Vega 64)

- Graphics Core
- Shader Engine
- Shader Array
- CU
- I$ and K$
- L1$
- L2$
- Scalable Data Fabric
- GDDR6
Memory Hierarchy - L2 Clients

- On the Polaris architecture only the CUs are clients of L2. Copy Engine, CP and Render Backend directly write to memory.
  → Lots of L2 flushes.
Memory Hierarchy - L2 Clients

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- With the “Vega” architecture CP and the Render Backend became clients of L2. → Reduced number of L2 flushes. Uploads via copy queue still require an L2 flush.
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- With the “Vega” architecture CP and the Render Backend became clients of L2. → Reduced number of L2 flushes. Uploads via copy queue still require a flush.

- On RDNA the Copy Engine is now a client of L2, too. → You should rarely observe a L2 flush on “Navi”.

[Diagram showing the memory hierarchy with L2$ at the top, L1$ in the middle, and L2$ at the bottom, with nodes labeled Copy, CP, RB, and WGP.]
### Caches – Some numbers

<table>
<thead>
<tr>
<th></th>
<th>RX Vega 64</th>
<th>Size</th>
<th>Cache Line Size</th>
<th>Read/Write</th>
</tr>
</thead>
<tbody>
<tr>
<td>Instruction Cache (I$)</td>
<td>32KB per 4 CUs</td>
<td>32B</td>
<td>Read-only</td>
<td></td>
</tr>
<tr>
<td>Scalar Cache (K$)</td>
<td>16KB per 4 CUs</td>
<td>32B</td>
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⇒ Twice as much I$ and K$, balancing out requirement for twice as many scalar resources
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</tr>
<tr>
<td>L1 Cache</td>
<td>16KB per CU</td>
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</tr>
<tr>
<td>L0 Cache</td>
<td>2x 16KB per WGP (~2CUs)</td>
<td>128B</td>
<td>Read-only</td>
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→ Twice as much I$ and K$, balancing out requirement for twice as many scalar resources
→ Higher bandwidth due to 128B cache lines. Fills up the chip with fewer memory requests.
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<td>L1 Cache</td>
<td>16KB per CU</td>
<td>64B</td>
<td>Read-only</td>
<td></td>
</tr>
<tr>
<td>L2 Cache</td>
<td>4MB</td>
<td>64B</td>
<td>Read/Write</td>
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<td></td>
</tr>
<tr>
<td>L1 Cache</td>
<td>128KB per shader array</td>
<td>128B</td>
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<td></td>
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- Twice as much I$ and K$, balancing out requirement for twice as many scalar resources
- Higher bandwidth due to 128B cache lines. Fills up the chip with fewer memory requests.
- Lower latency over “Vega” due to 512KB additional caches (L1).
<table>
<thead>
<tr>
<th></th>
<th>“Vega”</th>
<th>“Navi”</th>
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<tbody>
<tr>
<td></td>
<td>Compressed Reads</td>
<td>Compressed Writes</td>
</tr>
<tr>
<td>CU</td>
<td>✔️</td>
<td>✗️</td>
</tr>
<tr>
<td>Render Backend</td>
<td>✔️</td>
<td>✔️</td>
</tr>
<tr>
<td>Present Queue</td>
<td>✗️</td>
<td>N/A</td>
</tr>
</tbody>
</table>

→ Decompression barrier before writing to UAV.

→ Decompression barrier before Present.

→ Expect more textures to stay compressed.
→ Compute all the things!
DCC Everywhere

- On “Vega”:

- On “Navi”:

→ Bandwidth to VMEM stays unaffected.
DCC Everywhere – Compressed Writes

- Scattered Write

- 256B Coalesced Write
  (4bpp in Wave64, 8bpp on Wave32)

→ Prefer coalesced stores of at least 256B per wave for full efficiency.
→ Good rule of thumb: Write 8x8 blocks to images with 8x8 workgroup size.
Back to the WGP – Texture Units
### Texture Unit - Changes to TA/TD

<table>
<thead>
<tr>
<th>Feature</th>
<th>GCN</th>
<th>RDNA</th>
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<td>Load addressing</td>
<td>4 to 16 (coalesced) addresses/clk</td>
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<tr>
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→ Easier to reach maximum bandwidth via loads.
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→ Easier to reach maximum bandwidth via loads.
→ Easier to reach maximum bandwidth via stores.
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<tr>
<td>Filtering 64bit texels</td>
<td>2 components/clk</td>
<td>4 components/clk</td>
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</table>

- Easier to reach maximum bandwidth via loads.
- Easier to reach maximum bandwidth via stores.
- Improve FP16 with full rate 4 channel sampling.
Load / Store Queue – “Vega”

```assembly
...  
buffer_store_dword v2, v0, s[12:15], 0 idxen  
buffer_load_dword v0, v1, s[8:11], 0 idxen  
s_waitcnt vmcnt(0)  
v_add_f32 v0, v2, v0
```
Vector stores and loads increment VMCNT.

... 
buffer_store_dword v2, v0, s[12:15], 0 idxen  
buffer_load_dword v0, v1, s[8:11], 0 idxen  
s_waitcnt vmcnt(0)  
v_add_f32 v0, v2, v0 

VMCNT

1
Load / Store Queue – “Vega”

```assembly
... buffer_store_dword v2, v0, s[12:15], 0 idxen
buffer_load_dword v0, v1, s[8:11], 0 idxen
s_waitcnt vmcnt(0)
v_add_f32 v0, v2, v0
VMCNT
2
```
Load / Store Queue – “Vega”

\[
\text{...}
\text{buffer\_store\_dword v2, v0, s[12:15], 0 idxen}
\text{buffer\_load\_dword v0, v1, s[8:11], 0 idxen}
\text{s\_waitcnt vmcnt(0)}
\text{v\_add\_f32 v0, v2, v0}
\text{Wait here until VMCNT is 0.}
\]
Load / Store Queue – “Vega”

```
...  
buffer_store_dword v2, v0, s[12:15], 0 idxen  
buffer_load_dword v0, v1, s[8:11], 0 idxen  
s_waitcnt vmcnt(0)  
v_add_f32 v0, v2, v0
```

That means we also wait for the store!
Load / Store Queue – “Vega”

```assembly
...  
buffer_store_dword v2, v0, s[12:15], 0 idxen  
buffer_load_dword v0, v1, s[8:11], 0 idxen  
s_waitcnt vmcnt(0)  
v_add_f32 v0, v2, v0
```

VMCNT

0
Load / Store Queues - RDNA

```
... buffer_store_dword v2, v0, s[12:15], 0 idxen
buffer_load_dword v0, v1, s[8:11], 0 idxen
s_waitcnt vmcnt(0)
v_add_f32 v0, v2, v0
s_waitcnt vscnt(0)
s_barrier
```

“Navi” adds a separate queue for stores.
Load / Store Queues - RDNA

... buffer_store_dword v2, v0, s[12:15], 0 idxen
buffer_load_dword v0, v1, s[8:11], 0 idxen
s_waitcnt vmcnt(0)
v_add_f32 v0, v2, v0
s_waitcnt vscnt(0)
s_barrier

Stores increment VSCNT.

VMCNT | VSCNT
--- | ---
0 | 1
Load / Store Queues - RDNA

... buffer_store_dword v2, v0, s[12:15], 0 idxen
buffer_load_dword v0, v1, s[8:11], 0 idxen
s_waitcnt vmcnt(0)
v_add_f32 v0, v2, v0
s_waitcnt vscnt(0)
s_barrier

Loads still increment VMCNT.
Load / Store Queues - RDNA

... 
buffer_store_dword v2, v0, s[12:15], 0 idxen
buffer_load_dword v0, v1, s[8:11], 0 idxen
s_waitcnt vmcnt(0)
v_add_f32 v0, v2, v0
s_waitcnt vscnt(0)
s_barrier

Wait until all loads return and VMCNT drops to 0.
Load / Store Queues - RDNA

```assembly
...  
buffer_store_dword v2, v0, s[12:15], 0 idxen  
buffer_load_dword v0, v1, s[8:11], 0 idxen  
s_waitcnt vmcnt(0)  
v_add_f32 v0, v2, v0  
s_waitcnt vs cnt(0)  
s_barrier
```

Now we don’t wait for the store to finish!

![VMCNT: 0, VSCNT: 1]
Load / Store Queues - RDNA

... buffer_store_dword v2, v0, s[12:15], 0 idxen
buffer_load_dword v0, v1, s[8:11], 0 idxen
s_waitcnt vmcnt(0)
v_add_f32 v0, v2, v0
s_waitcnt vscnt(0)
s_barrier

Waiting for the store happens here.

VMCNT
0

VSCNT
1

Waiting for the store happens here.
... buffer_store_dword v2, v0, s[12:15], 0 idxen
buffer_load_dword v0, v1, s[8:11], 0 idxen
s_waitcnt vmcnt(0)
v_add_f32 v0, v2, v0
s_waitcnt vscnt(0)
s_barrier

We are good to go once the store operation returns.
Load / Store Queues - RDNA

- Optimization for the general case.
  - It’s very likely that you will see s_waitcnt vscnt(0) only in front of a s_barrier or in front of atomic operations.
  - s_endpgm implicitly waits on all counters.
- Non atomic stores are now true “fire and forget”.

```assembly
... buffer_store_dword v2, v0, s[12:15], 0 idxen
buffer_load_dword v0, v1, s[8:11], 0 idxen
s_waitcnt vmcnt(0)
v_add_f32 v0, v2, v0
s_waitcnt vscnt(0)
s_barrier
```
Load / Store Queues - RDNA

Effectively sequences like this will now run faster by default.

→ You might want to consider interleaving loads and stores again.

→ This has the additional benefit of saving VGPRs.

```assembly
buffer_load_dword v1, v0, s[4:7], 0 idxen
v_add_u32 v2, 1, v0
s_waitcnt vmcnt(0)
buffer_store_dword v1, v0, s[8:11], 0 idxen
buffer_load_dword v1, v2, s[4:7], 0 idxen
v_add_u32 v3, 2, v0
s_waitcnt vmcnt(0)
buffer_store_dword v1, v2, s[8:11], 0 idxen
buffer_load_dword v1, v3, s[4:7], 0 idxen
v_add_u32 v2, 3, v0
s_waitcnt vmcnt(0)
buffer_store_dword v1, v3, s[8:11], 0 idxen
buffer_load_dword v1, v2, s[4:7], 0 idxen
v_add_u32 v3, 4, v0
s_waitcnt vmcnt(0)
buffer_store_dword v1, v2, s[8:11], 0 idxen
buffer_load_dword v1, v3, s[4:7], 0 idxen
v_add_u32 v2, 5, v0
s_waitcnt vmcnt(0)
buffer_store_dword v1, v3, s[8:11], 0 idxen
buffer_load_dword v1, v2, s[4:7], 0 idxen
v_add_u32 v3, 6, v0
s_waitcnt vmcnt(0)
buffer_store_dword v1, v2, s[8:11], 0 idxen
buffer_load_dword v1, v3, s[4:7], 0 idxen
v_add_u32 v2, 7, v0
s_waitcnt vmcnt(0)
buffer_store_dword v1, v3, s[8:11], 0 idxen
buffer_load_dword v1, v2, s[4:7], 0 idxen
```
RDNA Fast Loads

- Texture Unit has low latency path for Loads.

- In general we need to keep the order with respect to Samples.

- Worst-case: Loads are as slow as Samples.

→ Replace all `texture.Sample(PointSampler, texcoord)` with `texture.Load(location)`!

→ Separate Loads and Samples if feasible.
Memory Hierarchy – Take Away

- 128B cache lines
  → You may want to adjust your memory alignments

- Addition of L1 gives access to more cache
  → Easier to run at peak ALU

- Independent loads and stores
  → Faster by default and opportunity for VGPR savings

- Higher bandwidth via PCIe® 4, load in parallel via PCIe® and copy queue (SDMA) on L2
  → Stream all the things on the copy queue

- DCC everywhere
  → Fully overwrite 256B blocks on store.
  → Another reason to move to compute 😊
RDNA

- RDNA - An all new architecture
- Focus on graphics & latency
  - Reduced latency throughout the whole pipeline
  - Higher efficiency on many graphics workloads
- A new infrastructure
  - New memory, interconnect, etc.
  - New display controllers
- Available July 7th!
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