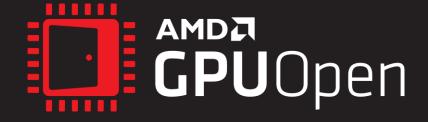


CONCURRENCY MODEL IN EXPLICIT GRAPHICS APIS

DOMINIK BAUMEISTER & DR. MATTHÄUS G. CHAJDAS



WHO WE ARE

Dr. Matthäus G. Chajdas 5 years at AMD Developer Technology Architect

Dominik Baumeister 3 years at AMD

Developer Technology Engineer





GOALS

- Give a (slightly) more in-depth look for people interested in graphics programming
- Prepare the mental model for explicit graphics APIs (DirectX12[®], Vulkan[®])

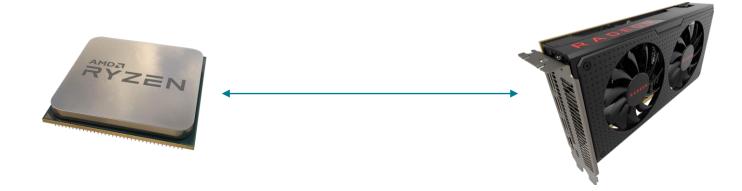






BASICS

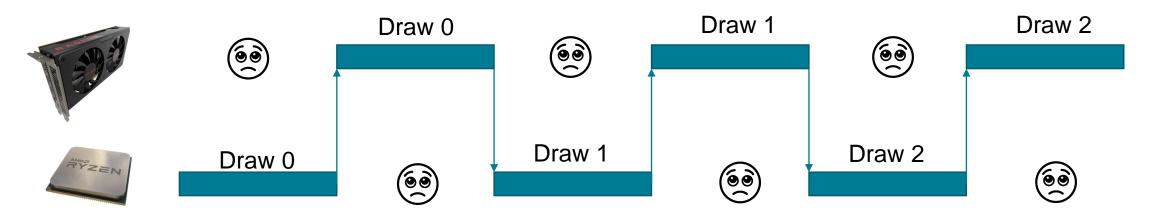
- Our program executes on the CPU
- Shaders can run as part of a Draw() or Dispatch() execution on the GPU
- CPU and GPU are physically separate entities (even in case of an integrated GPU, they're separate blocks on the chip)





NAIVE VIEW

 What would happen if a Draw() would be executed immediately on the GPU (i.e., like calling a function)

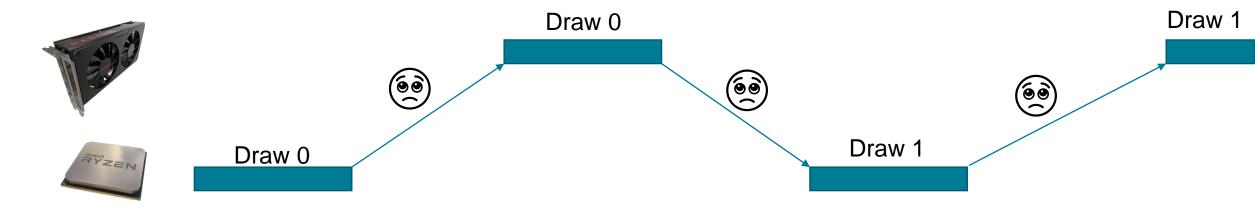


• Of course not what we would like to see



NAIVE VIEW

 In addition, "immediately" is actually "quite some time later" in practice as the commands have to be sent via a message across the bus





COMMAND RECORDING

- Instead: Keep most of the commands somewhere in memory
- Accumulate a lot of them (ideally enough to keep the GPU busy for a while)
- Then "Submit" them to the GPU



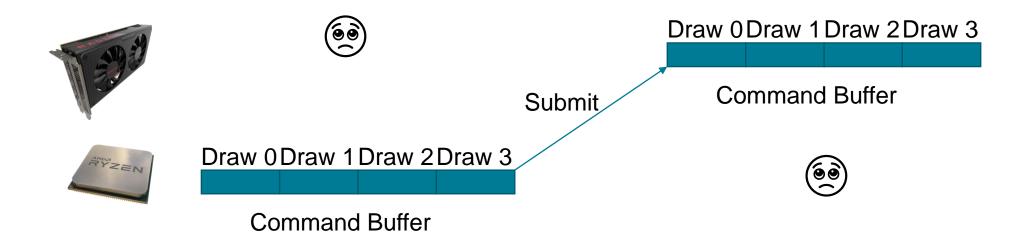
Draw 0Draw 1Draw 2Draw 3

Command Buffer



COMMAND RECORDING

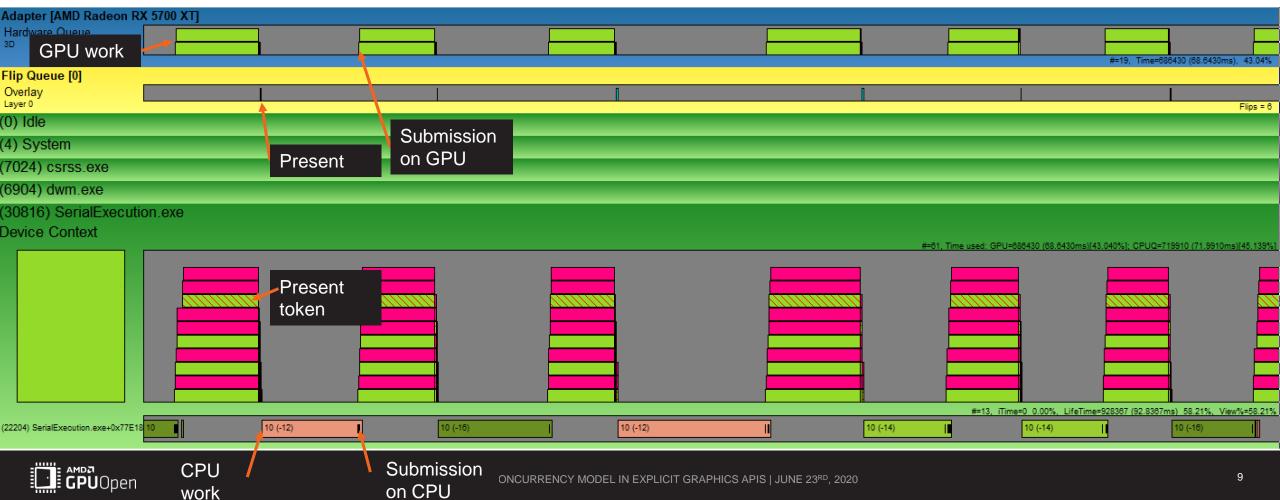
- Again, we're running into the same challenge (conceptually):
 - CPU is working hard to create the commands, meanwhile the GPU is idle
 - Then GPU is working hard to execute the commands, meanwhile the CPU is idle





SERIAL EXECUTION

How can I detect these cases? – GPUView (<u>https://graphics.stanford.edu/~mdfisher/GPUView.html</u>)



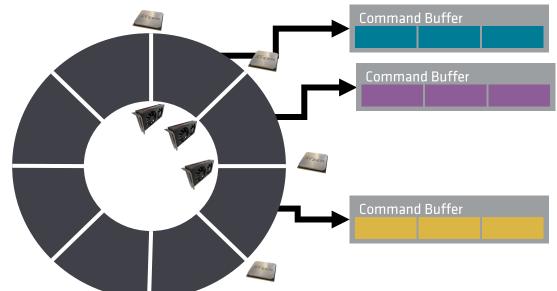
SERIAL EXECUTION

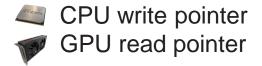
- Reminder: GPU and CPU are separate entities with their own timeline and resources. They don't necessarily run in sync!
- This means in practice you actually have to do additional work to sync them up (and thus to generate the pathological case shown before ③)



RING BUFFER

- The CPU tells the GPU where to find the commands in memory via a ring buffer
- The CPU can then move on to do some meaningful work while GPU executes the commands
- Possibly the CPU is submitting more command buffers, even though the GPU is still churning on the first one







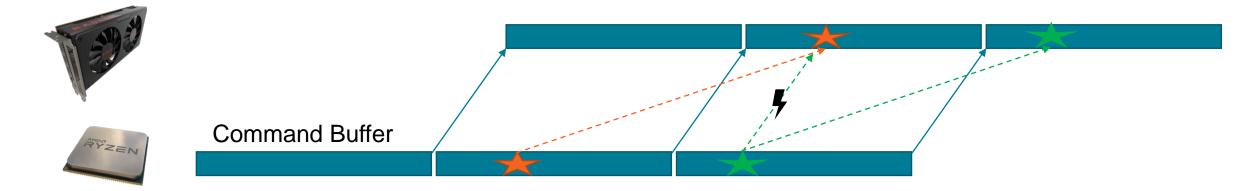
OVERLAPPING EXECUTION

In GPUView (<u>https://graphics.stanford.edu/~mdfisher/GPUView.html</u>)

Adapter [AMD Radeon I	RX 5700 XT]									
Hardware Queue										
Flip Queue [0]									#=33, Time=94812	21 (94.8121ms), 74.52%
Overlay Layer 0		1	1	1	1	1	1	1		
										Flips = 11
(0) Idle										
(4) System										
(7024) csrss.exe										
(6904) dwm.exe										
(29432) Overlappingl	Execution.exe									
Device Context										
				 			#=99, Time used	: GPU=948121 (94.8121ms	[74.525%]; CPUQ=100271	4 (100.2714ms)[78.816%]
							#=1,	iTime=0 0.00%, LifeTime	=1272223 (127.2223ms) 1	00.00%, View%=100.00%
(8116) OverlappingExecution.exe+0	0x771E0(812)				1			I	1	I



OVERLAPPING EXECUTION

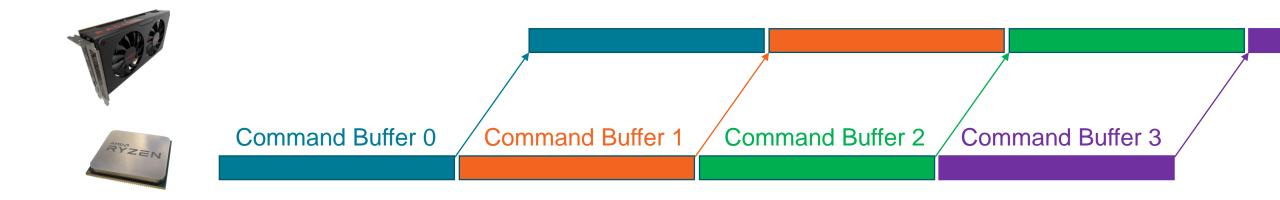


- Benefits: GPU and CPU can work in parallel
- Drawbacks:
 - Can't overwrite command buffers that are already in flight
 - Can't overwrite constants that are already in flight
 - Can't change/destroy textures and buffers that are currently in use



BUFFERING

• The solution is buffering





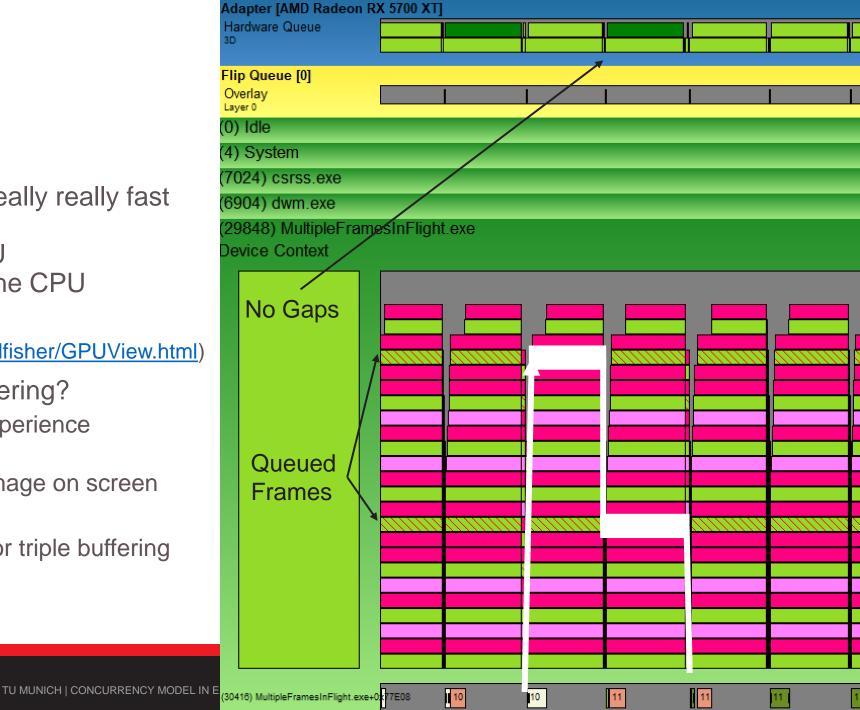
BUFFERING

- Keep multiple copies of your
 - Command buffers
 - Descriptors
 - Small objects that describe your buffers & textures
 - Memory address, size, mip level count, swizzle ...
 - Constant buffers
- Most of that is done for you on older APIs
- On recent, explicit APIs you are responsible to do that yourself



BUFFERING

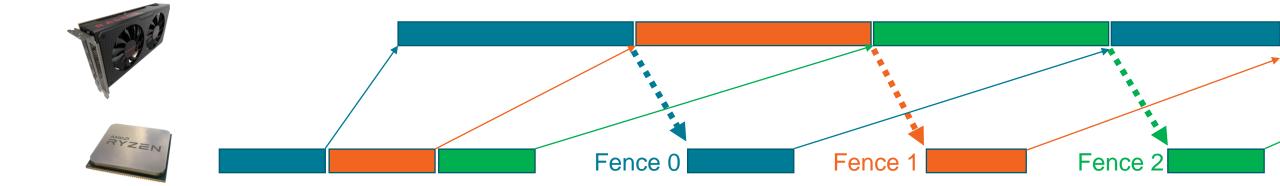
- Now suppose our CPU is really really fast or in more general terms: Executing work on the GPU takes a lot longer than on the CPU
- GPU View again (<u>https://graphics.stanford.edu/~mdfisher/GPUView.html</u>)
- Tripple (quadruple, ...) buffering?
 - Can help with smoother experience
 - At the expense of latency
 = time from user input to image on screen
 - Can't do this forever
 - Usually games do double or triple buffering





SYNCHRONIZATION - FENCES

- At some point we need to know when the GPU has finished executing some work
- This is done via Fences
- If done correctly ~ once a frame this does not cause serial bottlenecks





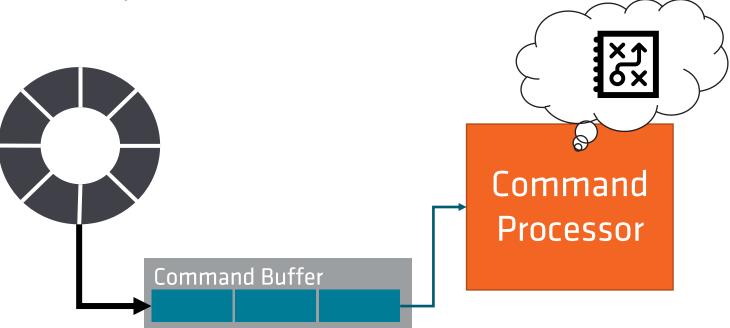
READBACK

- Now: What should we do if we want to read data from GPU memory on the CPU?
 - Screenshots
 - Timestamps for profiling
 - Occlusion queries (ever wondered where the white/black flashes in some games come from?)
- We don't want to sync with the latest frame, this would bring us back to square one = CPU and GPU running serialized
- Instead, the CPU should continue performing useful work and periodically poll the GPU when the frame is complete



COMMAND PROCESSOR

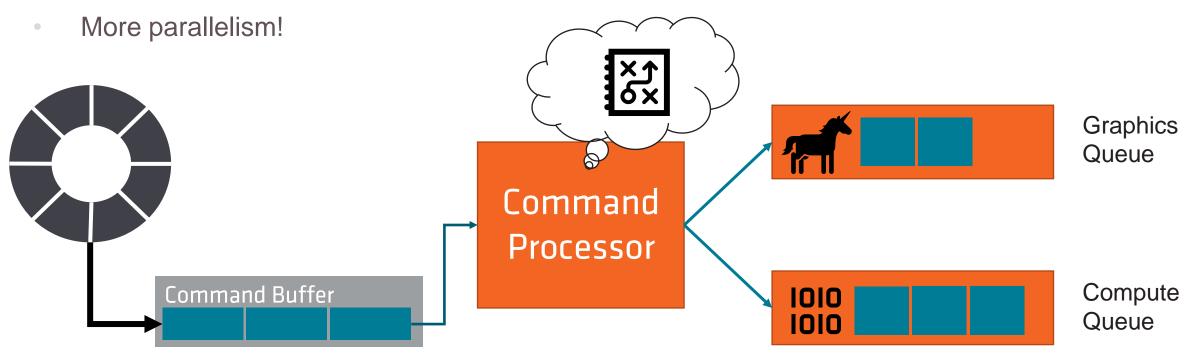
- Leaving the realm of the CPU, we're now **on the GPU**
- Reads the pointer to the command buffer from the ring buffer
- Interprets the commands in the stream





COMMAND PROCESSOR

- Schedules them for the respective queues
 - There are Graphics Queues
 - And Compute Queues





QUEUES

- Different synchronization domains
- But share the same ALUs, registers
- For that reason they are useful to overlap ALU heavy work with fixed function heavy work
- Two ALU limited workloads on different queues will likely not run faster than on a single queue
- But for example shadow map creation (rasterizer limited) and ambient occlusion (ALU limited) go hand in hand pretty well



QUEUES



			-						
	START	OVERVIEW EVENTS							
Frame summary		System activity							
Barriers		Visualize command buffer submission and s	ynchronization primitives.						
Most expensive events		r		mission markers				Zoom to selection Reset z	oom 🛛 🖨 👄
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Render/depth targets			Sequential						
Device configuration				·····					
		Graphics queue		1					
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		<							>

SEMAPHORES

- Again, somehow have to make sure that two queues can be synchronized: Done using Semaphores (Vulkan) or Fences (D3D12).
- Semaphores can be signalled and waited on
- They have some overhead both on CPU and GPU
 - GPU has to fill up again (from the very front of the pipeline)
 - OS on the CPU makes sure that you cannot deadlock the GPU i.e., avoid that one application can make the whole system unresponsive



SEMAPHORES



	Frame 5903 Detailed GPU events											Frame 59	05			
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[245249]								-	577] VkCommandBuffe	r						
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Compute queue

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[0x17e33bea110] VkSemaphoreWait	[242689] VkCommandBuffer	[0x17e33bea110] VkSemaphoreWait	[246017] VkCommandBu

>

SHADER CORE

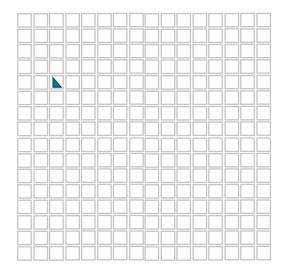
- Now to the actual execution in the shader core
- Loads of vector units (execute in lock step)
- Bunched up in Compute Units (execute independently from each other)
- "Dual Compute Unit" Radeon™ RX 5700 XT contains 20 of those → 2560 hardware threads in total

I\$ K\$	SALU	SIMD32	SALU	SIMD32		Texture Addresser	LO\$	
	5/(20	Shribbe	5/120	SILLESE		Texture Data	200	
					LDS			
	SALU	SIMD32	SALU	SIMD32		Texture Addresser	LO\$	
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SHADER CORE

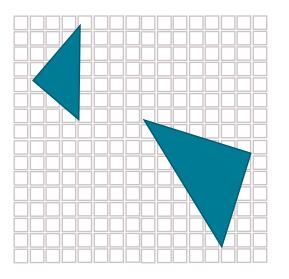
- For full utilization we want to avoid synchronous execution as much as possible.
- Imaging a huge GPU with thousands of ALUs and then your triangles cover a single pixel.
 99% of the GPU would idle.





PARALLEL EXECUTION

- APIs require draw calls to be issued in the order they have been submitted
- They also require the results to become visible in the order they have been submitted
- GPUs go to great lengths to execute in parallel while maintaining the illusion of serial execution
 - This can cause interesting (correct) behavior.
 - Imagine two triangles not overlapping: The later one can finish before the first.







BARRIERS

• Stalls execution until all remaining work on the same queue has been done.

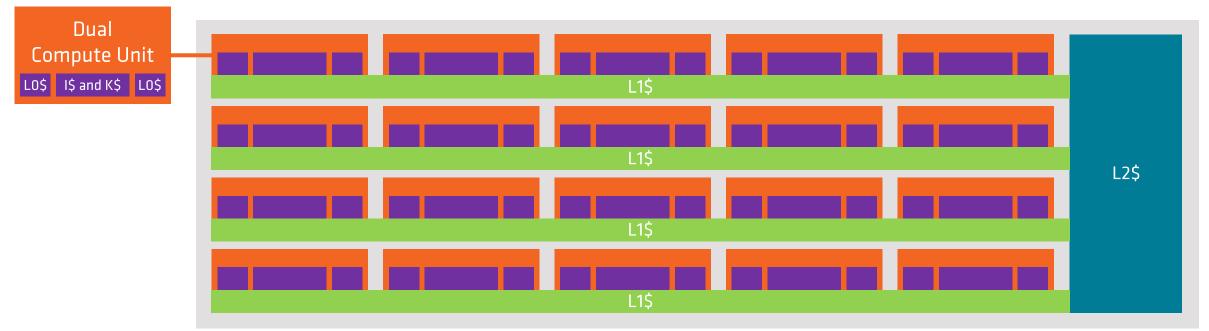


PS: This is bad practice, FidelityFX SPD (<u>https://gpuopen.com/fidelityfx-spd/</u>) shows how to do it better.



BARRIERS

- Handle visibility operations
 - i.e., possibly insert cache flushes to make contents of L0 caches visible to other compute units

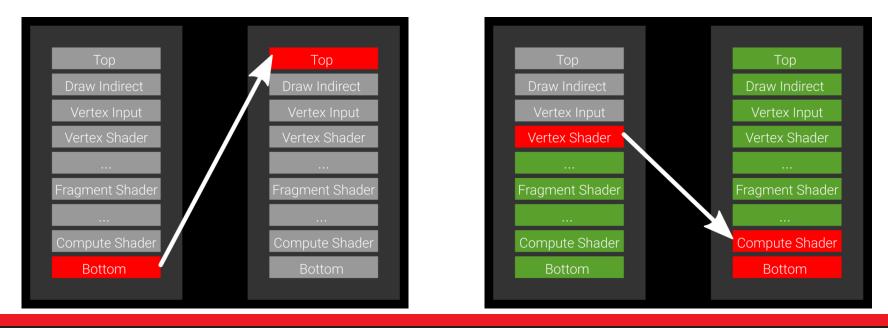


Cache Hierarchy Radeon[™] RX 5700 XT (simplified)



BARRIERS

- There is more parallelism: the Graphics Pipeline is well... a pipeline
- The different stages for a Draw/Dispatch run (partly) in serial, but new work can already start while old work items are still being executed
- More on GPUOpen: <u>https://gpuopen.com/learn/vulkan-barriers-explained/</u>





FURTHER READS

- Lots of relevant information on GPUOpen <u>https://gpuopen.com</u>
- Including practical tools like the Radeon GPU Profiler <u>https://gpuopen.com/rgp/</u>
- RDNA <u>https://gpuopen.com/documentation/</u>

GPUOpen

- Keeping your GPU fed without getting bitten <u>https://www.khronos.org/assets/uploads/developers/library/2017-khronos-uk-vulkanised/004-Synchronization-Keeping%20Your%20Device%20Fed_May17.pdf</u>
- Breaking down Barriers <u>https://therealmjp.github.io/posts/breaking-down-barriers-part-1-whats-a-barrier/</u>
- A trip through the graphics pipeline https://fgiesen.wordpress.com/2011/07/09/a-trip-through-the-graphics-pipeline-2011-index/
- GPU View <u>https://graphics.stanford.edu/~mdfisher/GPUView.html</u>



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AMD Radeon FreeSync requires a monitor and AMD Radeon™ graphics, both with FreeSync support. Seewww.amd.com/freesync for complete details. Confirm capability with your system manufacturer before purchase. GD-127

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